

METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A  
MEMORY FROM BEHAVIORAL DESCRIPTIONS

ABSTRACT

5           A method and system for constructing a structural model of a memory  
for use in ATPG (Automatic Test Pattern Generation). According to an  
embodiment of the present invention, behavioral models of memories of the  
simulation libraries are re-coded into simplified behavioral models using  
behavioral hardware description language (e.g., Verilog). Then, the  
10   simplified behavioral models are automatically converted into structural  
models that include ATPG memory primitives. The structural models are  
then stored for subsequent access during pattern generation. In one  
embodiment, for modeling random access memories (RAMs), the ATPG  
memory primitives include memory primitives, data bus primitives, address  
15   bus primitives, read-port primitives and macro output primitives. In  
another embodiment, for modeling content addressable memories (CAMs),  
the ATPG memory primitives include memory primitives, compare port  
primitives and macro output primitives. An advantage of the present  
invention is that functional equivalence between the simplified behavioral  
20   models and the simulation models can be easily verified with the same  
behavioral hardware description language simulator (e.g., Verilog simulator).  
Another advantage of the present invention is that very complicated  
memories, such as CAMs, can be accurately modeled for ATPG.